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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/736,244	12/15/2003	Chia Yong Poo	2269-4885.1US (01-0253.01	6438

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/736,244	POO ET AL.	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/18/05*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) *3,11 and 13-53* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,8-10 and 12* is/are rejected.

7)☒ Claim(s) *6 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/1/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/736244 Attorney's Docket #: 2269-4885.1US01-0252.01/US
Filing Date: 12/15/2003; claimed foreign priority to 6/2/2002

Applicant: Poo et al.

Examiner: Alexander Williams

Applicant's Amendment filed 7/18/05 to the election without traverse of species 3, subspecies 3B of Applicant's detailed species listing of figures 7, 11 and 14 (claims 1 to 45), filed 10/1/2004, has been acknowledged. However, claims 3, 11 and 13-45 DO NOT READ on the elected species of figures 7, 11 and 14, therefore will NOT be examined at this time. Claims 1, 2, 4-10 and 12 DOES READ on the elected species and will now be examined.

This application contains claims 3, 11 and 13-45 drawn to an invention non-elected without traverse.

This application contains claims 46 to 52 drawn to an invention non-elected without traverse.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of

the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 2, 4, 5, 8-10 and 12 are rejected under 35 U.S.C. § 102(b) as being anticipated by Kowase (Japan Patent # 63-232342).

1. Kowase (figures 1 to 7) specifically figures 5 and 6 show a semiconductor device package, comprising: a semiconductor device **1** including at least one bond pad **(2 within 1 at the top surface)** on an active surface **(top of 1)** thereof and at least one recess **13** in a peripheral edge thereof; at least one outer connector **18** corresponding to the at least one bond pad, the at least one outer connector positioned at least partially within the at least one recess and having a height that extends substantially along a height of the peripheral edge; and at least one conductive trace **14** extending between the at least one bond pad and the at least one outer connector.

2. The semiconductor device package of claim 1, Kowase further comprising: an insulative layer (4 within 1) positioned beneath at least the at least one conductive trace.

4. The semiconductor device package of claim 1, Kowase further comprising: a back side insulative layer (4 within 1 bottom) substantially covering a back side of the semiconductor device.

5. The semiconductor device package of claim 1, Kowase show wherein the at least one outer connector comprises opposite surfaces exposed at the active surface and a back side of the semiconductor device.

8. The semiconductor device package of claim 1, Kowase show comprising a plurality of outer connectors.

9. The semiconductor device package of claim 8, Kowase show comprising a plurality of conductive traces **14** that corresponds to at least some of the plurality of outer connectors.

10. The semiconductor device package of claim 9, Kowase show wherein each of the plurality of conductive traces establishes electrical communication between a bond pad of the semiconductor device and a corresponding outer connector of the plurality of

outer connectors.

12. The semiconductor device package of claim 8, Kowase show wherein outer connectors of the plurality of outer connectors are positioned adjacent to at least two peripheral edges of the semiconductor device.

ABSTRACT:

PURPOSE: To eliminate bonding wires and a wire bonding process and reduce the area of a semiconductor chip by a method wherein outer terminals on the side surfaces of the semiconductor chip are contacted with inner terminals of the leads on the side surfaces of the recess of a package in which the chip is housed.

CONSTITUTION: If a semiconductor chip 1 is inserted into the recess 7 of a package 6 to contact the respective wiring terminals 3 of the chip 1 with the leads 8 and 9 of the package 6 on the side surfaces of the chip 1 in such a manner that no gap exists between the chip 1 and the package 6, the conductive layers 3 on the side surfaces of the chip 1 and the conductive layers 8 and 9 on the side surfaces of the recess 7 are tightly contacted with each other and electrical connection can be obtained. With this constitution, wire bonding between the chip and package can be eliminated so that simplification and automation of packaging can be realized.

Claims 1, 2, 4, 5, 8-10 and 12 are rejected under 35 U.S.C. § 102(b) as being anticipated by Akram et al. (U.S. Patent # 6,072,236).

1. Akram et al. (figures 1 to 10) specifically figures 6 and 7 show a semiconductor device package **210**, comprising: a semiconductor device including at least one bond pad **116,16** on an active surface thereof and at least one recess **22** in a peripheral edge thereof; at least one outer connector **122** corresponding to the at least one bond pad, the at least one outer connector positioned at least partially within the at least one recess and having a height that extends substantially along a height of the peripheral edge; and at least one conductive trace **16** extending between the at least one bond pad and the at least one outer connector.

2. The semiconductor device package of claim 1, Akram et al. further comprising: an insulative layer positioned beneath at least the at least one conductive trace.

4. The semiconductor device package of claim 1, Akram et al. further comprising: a back side insulative layer substantially covering a back side of the semiconductor device.
5. The semiconductor device package of claim 1, Akram et al. show wherein the at least one outer connector comprises opposite surfaces exposed at the active surface and a back side of the semiconductor device.
8. The semiconductor device package of claim 1, Akram et al. show comprising a plurality of outer connectors.
9. The semiconductor device package of claim 8, Akram et al. show comprising a plurality of conductive traces that corresponds to at least some of the plurality of outer connectors.
10. The semiconductor device package of claim 9, Akram et al. show wherein each of the plurality of conductive traces establishes electrical communication between a bond pad of the semiconductor device and a corresponding outer connector of the plurality of outer connectors.
12. The semiconductor device package of claim 8, Akram et al. show wherein outer connectors of the plurality of outer connectors are positioned adjacent to at least two peripheral edges of the semiconductor device.

(16) In yet another variation of the invention, the blank may be micromachined with a number of mutually parallel, extended grooves along and perpendicular to one edge of the package. The grooves, which may communicate directly with the bond pads of the die, or with rerouting traces on the face side of the die or the back side of the blank extending from original bond pad locations to new ones along one edge of the package, may be conductively coated to function as connectors when the package is "plugged" transversely into a carrier having slots with mating conductive clips or other elements to receive and connect to the die of the package in a DDC assembly. Alternatively, the trenches may function merely as alignment elements for the clips, which contact the new bond pads associated with the trenches.

Claims 6 and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response

Applicant's arguments filed 7/18/05 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The insertion of Applicant's additional claimed language, for example, "in claim 1 " cause for further search and consideration to make this action final.

Applicant's amendment necessitated the new grounds of rejection. Accordingly, **THIS ACTION IS MADE FINAL**. See M.P.E.P. ∋ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. ∋ 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. ∋ 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

The listed references on USPTO form 892 are cited as of interest to this application.

Field of Search	Date
U.S. Class and subclass: 257/777,686,685,690-693,696,698,673,666,684,796,784,786,787 361/777	4/11/05 9/21/05

174/262,257,52.4,52.2	
Other Documentation: foreign patents and literature in 257/	4/11/05 9/21/05
Electronic data base(s): U.S. Patents EAST	4/11/05 9/21/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
9/22/05

Primary Patent Examiner
Alexander O. Williams